REMARKS

The outstanding Office Action objects to claims 8, 17, 19, 26, and 33 due to claim informalities and rejects claims 1-38 under 35 U.S.C. §103(a) as being unpatentable over Bartley (U.S. Patent No. 6,219,796) in view of Fletcher et al. (U.S. Patent No. 6,611,920).

Claims 1, 8, 9, 17, 19, 26, 33, and 37 have been amended to further clarify the subject matter regarded as the invention. Claim 27 has been canceled. New claim 39 has been added. Claims 1-26 and 28-39 are now pending in this application.

Reconsideration of the application is respectfully requested based on the amendments and the following remarks.

CLAIM OBJECTIONS

Claims 8, 19, and 33 have been amended as suggested by the Examiner to correct the respective informalities.

Claims 17 and 26 have been amended to be distinct from each other.

REJECTION OF CLAIMS 1-38 UNDER 35 U.S.C. §103

The present invention pertains to methods and systems for saving power in pipelined processors. Specifically, claim 1 of the present invention requires the controlling of the supply of current to each of a plurality of stages of a functional unit immediately after the steps of evaluating instructions and producing activity indicators, which facilitate the control of the supply of current. The method of claim 1 allows for efficient evaluation of each instruction type so that power supplied to each stage of a functional unit can be controlled.

Bartley attempts to reduce power consumption by a processor by scanning program code for segments where a functional unit is not in use. Then power-related instructions are added to the program code to control the power supply to respective functional units. The power-related instructions are added manually by a programmer or by a compiler or assembler. See col. 7, lines 31-38. Since Bartley requires revising a program and then executing the revised program, Bartley fails to teach or suggest controlling the supply of current immediately after evaluating instructions and producing activity indicators, which are used to control the supply of current to respective stages of a functional unit.

It is understood that Fletcher et al. discloses a technique for controlling the power

supplied to individual stages of a functional unit block 310 that involves a valid indicator that passes through a propagation circuit. The valid indicator can be activated or deactivated, however, Fletcher et al. fails to teach or suggest when the status of the valid indicator would be decided. Therefore, Fletcher et al. fails to teach or suggest the controlling of the supply of current to each of a plurality of stages of a functional unit immediately after the steps of evaluating instructions and producing activity indicators, which facilitate the control of the supply of current. Therefore, it is submitted that Bartley and Fletcher et al., alone or in any combination, do not teach or suggest the features of claim 1.

Independent claim 9 and dependent claim 39 of the present invention pertain to methods that require receiving instructions at an instruction evaluation unit from an instruction register where the instruction evaluation unit evaluates the operation type of the instructions. The instruction register temporarily stores instructions before they are executed. The instructions of claims 9 and 39 are evaluated for their operation type shortly before being executed. In contrast, neither Bartley nor Fletcher et al. teach or suggest receiving instructions at an instruction evaluation unit from an instruction register where the instruction evaluation unit evaluates the operation type of the instructions. Therefore, it is submitted that Bartley and Fletcher et al., alone or in any combination, do not teach or suggest the features of claims 9 and 39.

Independent claims 17 and 37 pertain to a microprocessor and system where an instruction evaluation unit is connected to an instruction register where the instruction evaluation unit evaluates the next instruction to produce activity indicators. Furthermore, claims 17 and 37 recited that a stage activation controller is connected to the instruction evaluation unit, wherein the stage activation unit utilizes the activity indicators to activate or deactivate each stage of a functional unit. In contrast, neither Bartley nor Fletcher et al. teach or suggest an instruction evaluation unit that is connected to an instruction register where the instruction evaluation unit evaluates the next instruction to produce activity indicators. Also, neither Bartley nor Fletcher et al. teach or suggest a stage activation controller that is connected to the instruction evaluation unit. Therefore, it is submitted that Bartley and Fletcher et al., alone or in any combination, do not teach or suggest the features of claims 17 and 37.

Independent claim 26 pertains to a microprocessor that includes an AND gate having an input from a stage activation controller, an input from a clock circuit and an output to one of the stages of a functional unit. The AND gate presents a simple mechanism for controlling the supply of clock pulses to a respective stage. In contrast, neither Bartley nor Fletcher et al. teach or suggest an AND gate as recited in claim 26. Therefore, it is submitt d that Bartley and

Fletcher et al., alone or in any combination, do not teach or suggest the f atures of claims 26.

It is submitted that dependent claims 2-8, 10-16, 18-25, 28-36, 38-39 are also patentably distinct from Bartley and/or Fletcher et al. for at least the same reasons as those recited above for their corresponding independent claims. The additional limitations recited in the dependent claims are not further discussed, as the above-discussed limitations are believed to be sufficient to distinguish the claimed invention from the cited references. Thus, it is respectfully requested that the Examiner withdraw the rejection of claims 1-38 under 35 U.S.C § 103(a).

SUMMARY

It is respectfully submitted that all pending claims are allowable and that this case is now in condition for allowance. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

If any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 50-0388 (Order No. APL1P203).

Respectfully submitted,
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